TEXAS INSTRUMENTS

Low Dropout, Dual-Output Linear Regulator EVM Using the TPS70151

User's Guide

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Mixed-Signal Products

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Preface

About This Manual

This user's guide describes the TPS70151EVM–152 low dropout, dual-output evaluation module (SLVP152). The SLVP152 provides a convenient method for evaluating the performance of a dual-output linear regulator.

How to Use This Manual

- ❑ Chapter 1 Introduction
- ❑ Chapter 2 EVM Adjustments and Test Points
- ❑ Chapter 3 Circuit Design
- ❑ Chapter 4 Test Results

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

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The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- ❑ TPS70151 data sheets (literature number SLVS222)

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Tables

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Chapter 1

Introduction

This user's guide describes the TPS70151EVM–152 low dropout, dual-output evaluation module (SLVP152). LDOs provide ideal power supplies for rapidly transitioning DSP loads. The TPS701xx family of devices is designed to provide a complete power management solution for DSP, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any DSP applications with power sequencing requirement. Differentiated features, such as SVS supervisory circuit, manual reset inputs, and enable function, provide a complete system solution. Moreover, with its low quiescent current, low dropout voltage, low output noise, high PSRR, fast transient response, and high accuracy compared to standard LDOs, the TPS701xx provides an ideal solution where standard linear regulators are too inefficient or too slow and where a switch converter solution or the source power supply is too noisy.

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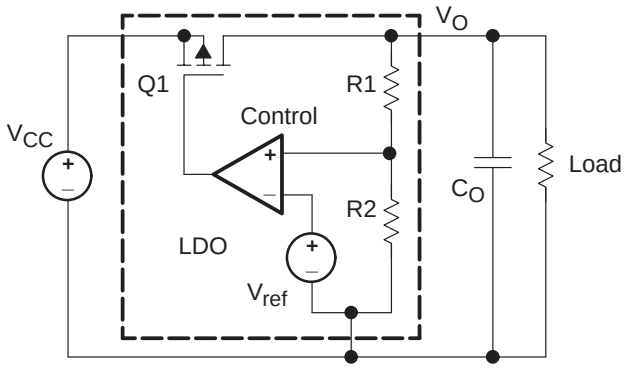
1.1 Low Dropout Voltage Linear Regulator Circuit Operation

In TI's low dropout voltage linear regulator topology, a PMOS transistor acts as the pass element. Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading.

The basic LDO regulator circuit includes the LDO and an output capacitor for stabilization. Figure 1–1 shows the circuit of a typical LDO application.

Figure 1–1. Typical LDO Application



In the LDO application shown in Figure 1–1, the LDO regulates the output voltage V_O.

If V_O falls below the regulation level, the controller increases the V_{SG} differential and the PMOS transistor conducts more current, resulting in an increase in V_O. If V_O exceeds the regulation level, the controller decreases the V_{SG} differential and the PMOS transistor conducts less current, resulting in a decrease in V_O. The PMOS pass element acts like an adjustable resistor. The more negative the gate becomes versus the source, the less the source-drain resistance becomes, resulting in higher current flow through the PMOS.

1.2 Design Strategy

The TI SLVP152 EVM provides a convenient method for evaluating the performance of TPS701xx dual-output linear regulators. The EVM provides proven, demonstrated reference designs and test modes to aid in evaluation. The board contains a power supply along with an onboard transient generator. The transient slew rate can be modified by changing two resistors. Jumpers allow settings of minimum/maximum load as well as device-enabling and power sequencing. There is enough room on the EVM to evaluate different types of output capacitors including ESR behaviors. Many test points allow the measuring of input, output, and dropout voltage.

The EVM contains a TPS70151. Regulator 1 provides an output voltage of 3.3 V and a maximum output current of 500 mA. Regulator 2 provides an output voltage of 1.8 V and a maximum output current of 250 mA.

Table 1–1 summarizes the TPS701xx family's features. See the TPS701xx datasheet, TI literature number SLVS222, for a further explanation of features.

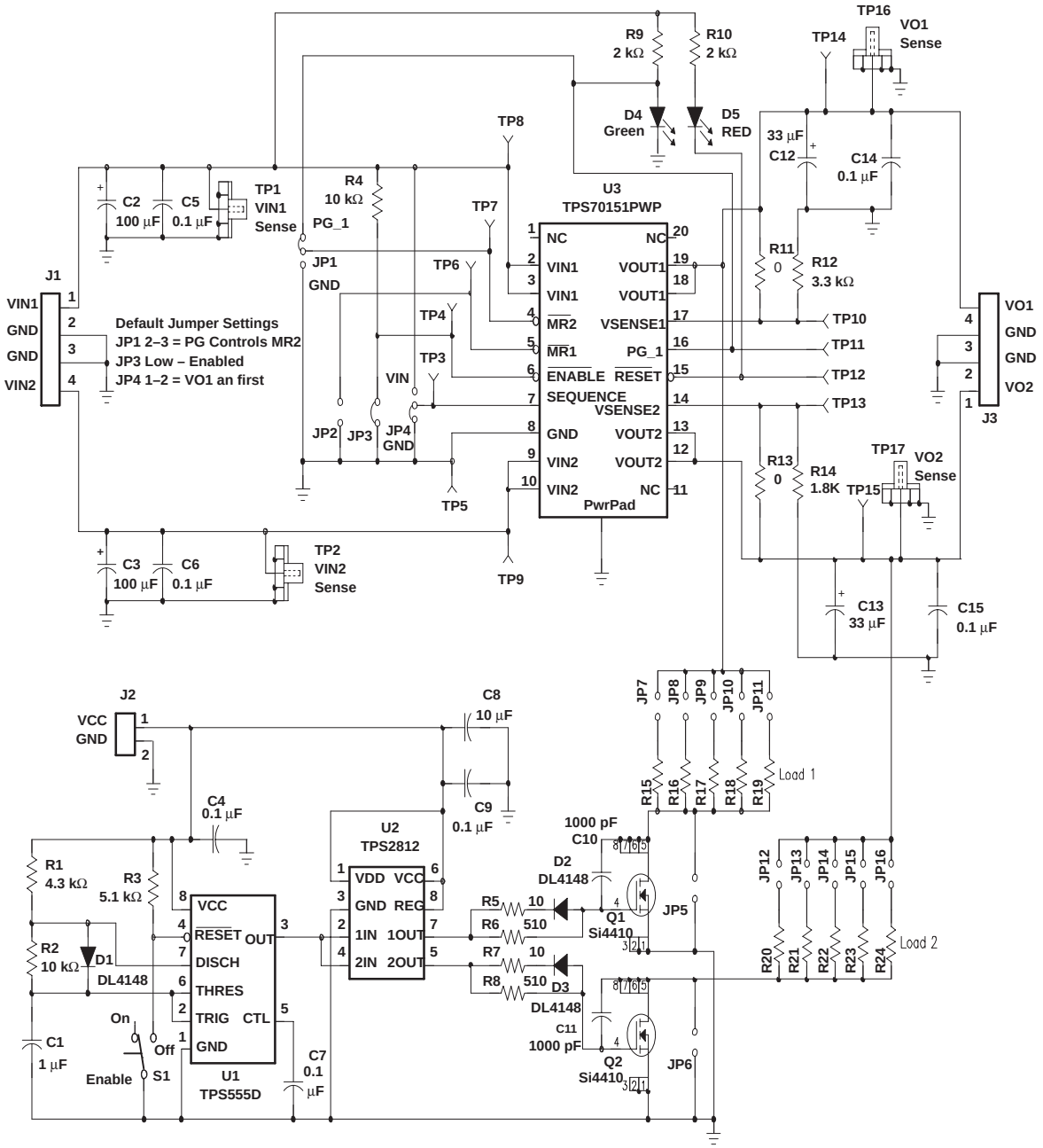
Table 1–1. Summary of the TPS701xx LDO Family Features

DESCRIPTION	TPS701xx FEATURE
Maximum input voltage [V]	6
Maximum output current [mA]	500/250
Typical quiescent current [μA]	190
Typical dropout voltage [mV]	150/200
Typical output noise [μVrms] (30 Hz ≤ f ≤ 50 kHz, C_O = 33 μF)	65
Accuracy over line, load, and temperature	2%
PSRR (at 1 kHz, C_O = 10 μF, T_J = 25°C)	80/60 dB
Package	PWP
Minimum output capacitor	> 10 μF (ceramic)
Available voltage option [V]	3.3/1.5, 3.3/1.2, 3.3/1.8, 3.3/2.5, and adj/adj
Performance advantage	Dual output LDO, power-up sequencing, DSP application, PG and RESET

1.3 Schematic

Figure1–2 shows the SLVP152 EVM schematic diagram.

Figure 1–2. SLVP152 EVM Universal LDO Tester Schematic Diagram



1.4 Bill of Materials

Table 1–2 lists materials required for the SLVP152 EVM.

Table 1–2. SLVP152 EVM Bill of Materials

Ref Des	Qty	Part Number	Description	MFG	Size
C1	1	ECJ-2VF1C105Z	Capacitor, ceramic, 1.0 uF, 16 V, 80% – 20%, Y5V	Panasonic	805
C4 – 7, 9, 14, 15	7	GRM39X7R104K016A	Capacitor, ceramic, 0.1 uF, 16 V, 10%, X7R	Murata	603
C2 – 3	2	TPSD107M010R100	Capacitor, tantalum, 100 μF, 10 V, 100-mΩ, 20%	AVX	D Case
C10, 11	2	GRM39X7R102K050A	Capacitor, Ceramic, 1000 pF, 50 V, 10%, X7R	Murata	603
C12, 13	2	10TPA33M	Capacitor, POSCAP, 33 μF, 10 V, 20%	Sanyo	D Case
C8	1	GRM235Y5V106Z016A	Capacitor, ceramic, 10 μF, 16 V, 80%–20%, Y5 V	TDK	1210
D1 – 3	3	DL4148	Diode, signal, 75 V, 200 mA	Diodes, Inc.	DL–35
D4	1	SML-LX2832GC-TR	Diode. LED, green, 2.1 V, 25 mcd, SM	Lumex	1210
D5	1	SML-LX2832RC-TR	Diode. LED, red, 1.7 V, 40 mcd, SM	Lumex	1210
J1, 3	2	ED1516	Terminal block, 4-pin, 6-A, 3.5 mm	OST	3.5 mm
J2	1	ED1514	Terminal block, 2-pin, 6A, 3.5 mm	OST	3.5 mm
JP1, 4	2	PTC36SAAN	Header, single-row, straight, 3-pin, 0.100” x 25 mil	Sullins	0.1”
JP2, 3, 5 – 16	14	PTC36SAAN	Header, single-row, straight, 2-pin, 0.100” x 25 mil	Sullins	0.1”
Shunts	16	929950-00-ND	Shunt, jumper, 0.1”	3M	0.1”
Q1, 2	2	Si4410DY	MOSFET, N-ch, 30-V, 10-A, 13 mΩ	Siliconix	SO–8
Q1,2 (Alt)		IRF7811	MOSFET, N-ch, 30-V, 10-mΩ	IR	SO–8
R1	1	Std	Resistor, chip, 4.3 kΩ, 1/16W, 5%		603
R2	1	Std	Resistor, chip, 10 kΩ, 1/16W, 5%		603
R3	1	Std	Resistor, chip, 5.1 kΩ, 1/16W, 5%		603
R4	1	Std	Resistor, chip, 10 kΩ, 1/16W, 5%		603
R5, 7	2	Std	Resistor, chip, 10 Ω, 1/16W, 5%		603
R6, 8	2	Std	Resistor, chip, 510 Ω, 1/16W, 5%		603
R9, 10	2	Std	Resistor, chip, 2.0 kΩ, 1/16W, 5%		603
R11, 13	2	Std	Resistor, chip, 0 Ω, 1/16W, 5%		603
R12	1	Std	Resistor, chip, 3.3 kΩ, 1/16W, 5%		603
R14	1	Std	Resistor, chip, 1.8 kΩ, 1/16W, 5%		603
R15 – 20	6		Resistor, chip, 33.2 Ω, 1 W, 1%		2512
R21 – 24	4		Resistor, chip, 51.1 Ω, 1 W, 1%		2512

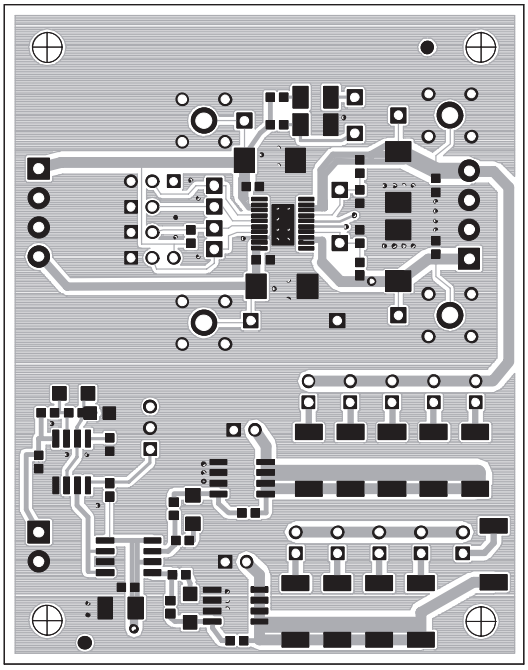
Table 1–2. SLVP152 EVM Bill of Materials (Continued)

Ref Des	Qty	Part Number	Description	MFG	Size
S1	1	EG1218	Switch, 1P2T, slide, PC-mount	E–Switch	0.1”
TP1, 2, 16, 17	4	131–4244–00	Adaptor, 3.5-mm probe clip (or 131–5031–00)	Tektronix	
TP3 – 15	13	240–345	Test point, red	Farnell	
U1	1	TLC555D	IC, timer	TI	SO8
U2	1	TPS2812D	IC, MOSFET driver, dual buffer	TI	SO8
U3	1	TPS70151PWP	IC, LDO regulator, dual-output	TI	PWP20
—	1	SLVP152, Rev. A	PCB, 2-layer, 2-oz, 3.10”(L) x 2.425”(W) x 0.062”(T)		

1.5 Board Layout

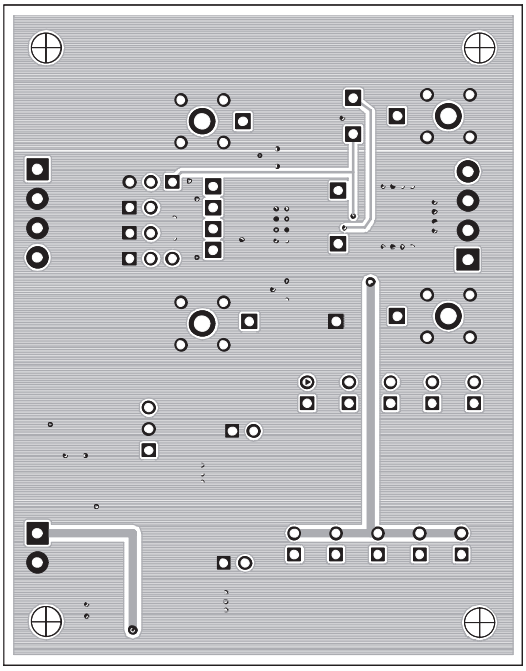
Figures 1–3 through 1-5 show the board layout for the SLVP125 EVM.

Figure 1–3. Top Layer



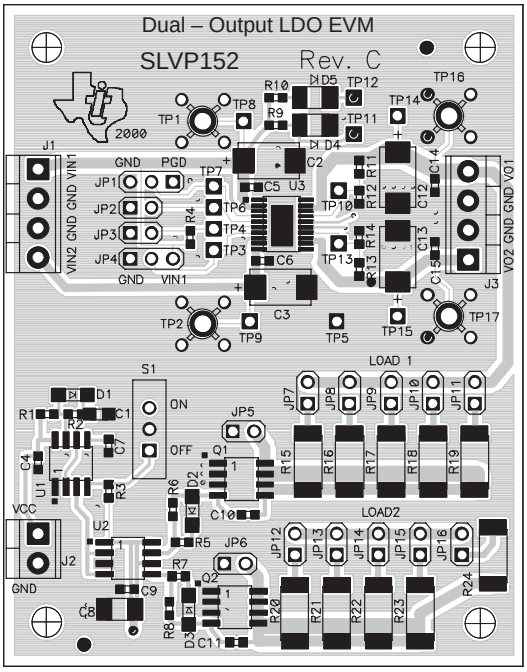
Top Layer

Figure 1–4. Bottom Layer (top view)



Bottom Layer (Top View)

Figure 1–5. Assembly Drawing (top assembly)



Top Assembly

Chapter 2

EVM Adjustments and Test Points

This chapter explains the following EVM adjustment modes:

- Adjustment by switch and jumper
- Adjustment through changing components

Figure 2–1 shows the locations of the adjustment points on the board.

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2.1 Adjustment by Switch and Jumpers

S1 switches the transient generator on or off. Table 2–1 lists adjustments that can be made by jumpers.

Table 2–1. Jumper Functions

Jumper	Setting	Functional Description
JP1	Short 1-2 – $\overline{\text{MR2}}$ tied to GND	$\overline{\text{RESET}}$ follows $\overline{\text{MR2}}$
	Short 2-3 – $\overline{\text{MR2}}$ tied to PG_1	$\overline{\text{RESET}}$ will go high after a 120 ms delay when V_{OUT2} reaches 95% of its regulated voltage and when PG_1 goes high due to V_{OUT1} reaching 95% of its regulated voltage.
	Open	$\overline{\text{MR2}}$ is disabled
JP2	Shorted – $\overline{\text{MR1}}$ tied to GND	$\overline{\text{RESET}}$ follows $\overline{\text{MR1}}$
	Open	$\overline{\text{MR1}}$ is disabled
JP3	Shorted – $\overline{\text{EN}}$ tied to GND	Enable DUT
	Open	Disable DUT
JP4	Short 1-2 – SEQ tied to GND	SEQ low – regulator 1 powers up first with regulator 2 powering up when V_{OUT1} is 83% of max output voltage.
	Short 2-3 – SEQ tied to V_{IN}	SEQ high or left open – regulator 2 powers up first with regulator 1 powering up when V_{OUT2} is 83% of max output voltage
JP5	Shorted – bypass transient generator for regulator 1	Allows continuous load through onboard load resistors on regulator 1.
	Open – engage transient generator for regulator 1	Allows pulsed load through onboard load resistors on regulator 1.
JP6	Shorted – bypass transient generator for regulator 2	Allows continuous load through onboard load resistors on regulator 2.
	Open – engage transient generator for regulator 2	Allows pulsed load through onboard load resistors on regulator 2.
JP7 – JP11	Shorted – include resistor in parallel combination	Increase regulator 1 load from no load to max load.
	Open – remove resistor from parallel combination	Decrease regulator 1 load from max load to no load.
JP12 – JP16	Shorted – include resistor in parallel combination	Increase regulator 2 load from no load to max load.
	Open – remove resistor from parallel combination	Decrease regulator 2 load from max load to no load.

The TPS701xx datasheet, TI Literature number SLVS222, provides further explanation of alternative configurations using the SVS supervisory circuit, power good, manual reset, and enable inputs.

2.2 Adjustment Through Component Changes

Through minor soldering work, the DUT can be changed to any of the fixed-voltage members of the TPS701xx LDO family. In addition, Table 2–2 summarizes the most common components which a user might wish to replace in order to more fully characterize the LDO.

Table 2–2. Commonly Changed Components

Component	Regulator 1	Regulator 2	EVM Value
Input capacitor	C2	C3	100 µF
Output capacitor	C12	C13	33 µF
Resistors controlling transient pulse generator pulse width and duty cycle (see Table 2-3)	R1, R2	R1, R2	4.3 kΩ, 10 kΩ
Resistor controlling load transient rise time†	R6	R8	510 Ω

† Larger resistance slows rise time.

Table 2–3 gives the equations for computing the resistor sizes necessary for changing the transient pulse width and/or duty cycle.

Table 2–3. Timing Equations

Timing Equations With Diode D1 for Low Duty Cycles	Timing Equations Without Diode D1
$R1 = \frac{t_{on}}{0.693 \times C}$	$R1 = \frac{t_{on} \times (2D - 1)}{0.693 \times D \times C}$
$R2 = \frac{t_{on} \times (1 - D)}{0.693 \times D \times C}$	$R2 = \frac{t_{on} \times (1 - D)}{0.693 \times D \times C}$

Note: t_{on} = desired load on-time [s]
D = on-time duty cycle
C = total capacitance in circuit (1 uF)
RH1, RH2 = Timer resistors value (refer to schematics) [Ω]

2.3 Test Setup

Figure 2–1 shows the test setup. Follow these steps for initial power up of the SLVP152

1) Adjust the settings of jumpers to fit test requirements (see jumper functions in Table 2-1). Verify that the switch controlling the load transient generator is off, no external load is connected through J3 and that JP5 and JP6 are open to prevent loading through the onboard resistors.

2) Connect a 12-V lab power supply to the V_{CC} input and GND at J2. The polarity is printed on the board. A current limit of 100 mA should be adequate for the test and measure circuit.

3) Connect a second lab power supply (at least capable of supplying 2 A) to the J1 connector at V_{IN1}, V_{IN2}, GND1 and GND2. The polarity is printed on the board. Verify that the lab power supply output voltage limit is set to 6 V and that the output is set to 0 V.

4) Turn on the 12-V lab supply. Turn on the second power supply and ramp the input voltage up to the desired maximum but not higher than 6 V.

5) Verify that the output voltage (measured at the V_{OUT1} and V_{OUT2} pins respectively) has the desired value.

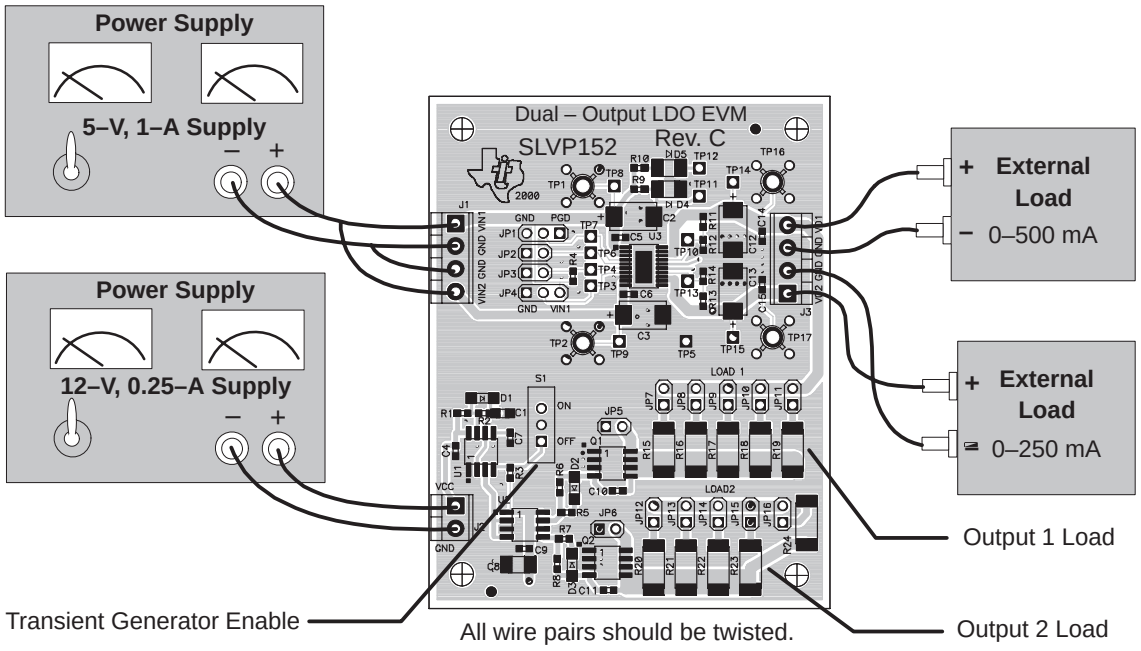
6) Table 2–4 shows the three recommended options for loading each regulator.

Table 2–4. Regulator Loading Options

Type	JP5–Regulator 1 JP6–Regulator 2	SW_1	External Load
Continuous load off-board	Open	Off	Connected
Continuous load onboard	Shorted	On/off	Not connected
Pulsed load onboard	Open	On	Not connected

Jumpers JP7 – JP11 and JP12 – JP16 vary the current through the onboard resistors from 0 to max load current for regulator 1 and regulator 2 respectively.

Figure 2–1. Test Setup



The PG_1 LED indicator (D4) has V_{on} = 2.1 V; therefore, for this test board, the maximum PG_1 output voltage (TP11) is 2.1 V. Since the PG_1 pin is an open drain, active high output terminal in a typical application, the PG_1 output could have a typical TTL range.

Chapter 3

Circuit Design

This chapter describes the LDO circuit design procedure.

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3.1 Temperature Considerations

To protect the device and assure the specifications, the maximum junction temperature should not exceed 125°C. If the temperature exceeds 150°C, thermal shutdown will turn off the device. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$. The maximum power dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{J,max} - T_A}{R_{\theta JA}}$$

Where:

- $T_{J,max}$ is the maximum allowed junction temperature [°C], i.e., 125°C for the TPS701xx families
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 32.6°C/W for the 20-terminal TSSOP package
- T_A is the ambient temperature

The regulator dissipation is calculated using:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT}$$

3.2 ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

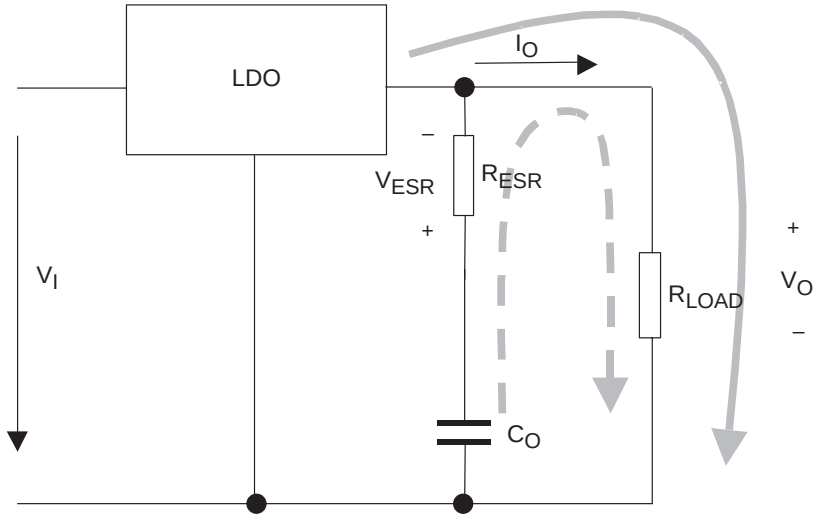
Besides its capacitance, every capacitor also contains parasitic impedances. These impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 3–1.

Figure 3–1. ESR and ESL

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

Figure 3–2 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

Figure 3–2. LDO Output Stage With Parasitic Resistances ESR



In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V(C_O) = V_O$). This means no current is flowing into or out of the C_O branch.

If I_O suddenly increases (transient condition), the LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 3–3). Therefore, capacitor C_O provides the current for the new load condition (dashed arrow). C_O now acts like a battery with an internal resistance, R_{ESR}. Depending on the current demand at the output, a voltage drop will occur at R_{ESR}. This voltage is shown as V_{ESR} in Figure 3–2.

When C_O is conducting current to the load, initial voltage at the load will be $V_O = V(C_O) – V_{ESR}$. Due to the discharge of C_O, the output voltage V_O will drop continuously until the response time t_1 of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 3–3.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

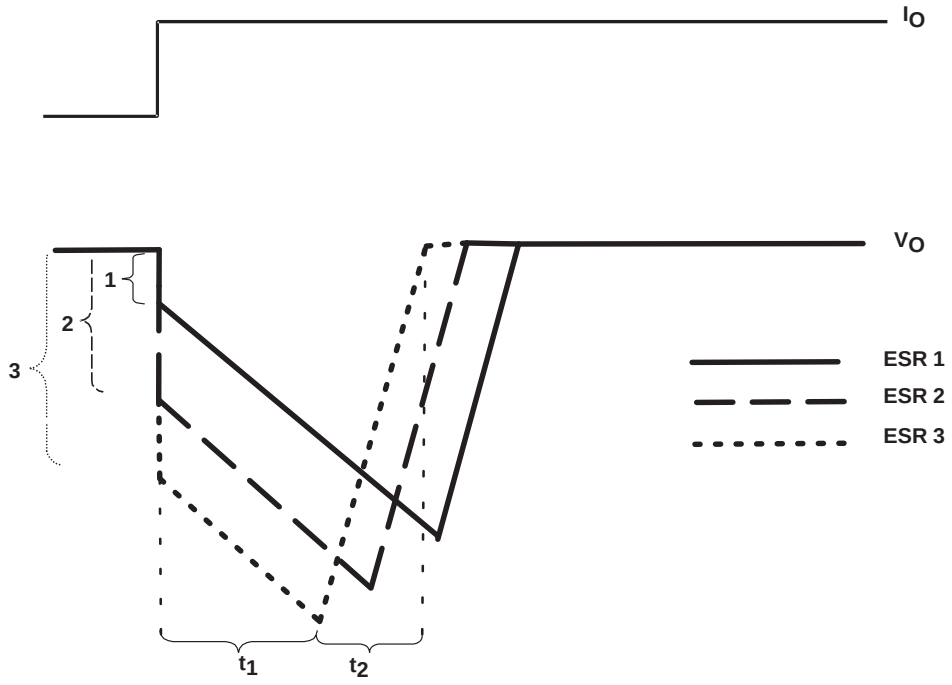
From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

3.2.1 Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement for a given LDO response time.

Figure 3–3. Correlation of Different ESRs and Their Influence to the Regulation of V_O at a Load Step From Low-to-High Output Current



Chapter 4

Test Results

This chapter presents laboratory test results for the TPS70151 LDO design.

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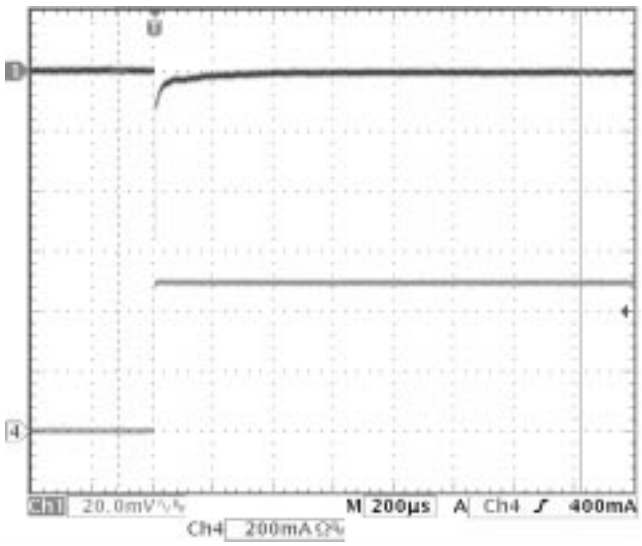
4.1 Test Results

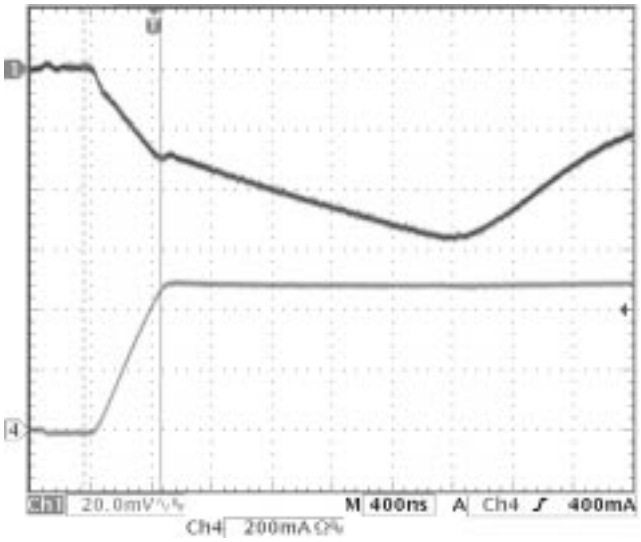
Figures 4–1 through 4–9 show the results of various test conditions using the TPS70151 device. In figures 4–1 through 4–3, channel 1 is regulator 1 output voltage and channel 4 is the load current. In figures 4–4 through 4–9, channel 1 is regulator 1 output, channel 2 is regulator 2 output, and channel 4 is $\overline{\text{RESET}}$. Channel 3 is PG_1 in figures 4–4 through 4–8. Channel 3 is $\overline{\text{MR1}}$ in figure 4–9.

Figure 4–1. No Load – Full Load (500 mA) Transition With C_O = 33 µF POSCAP™ – LDO Settling Time



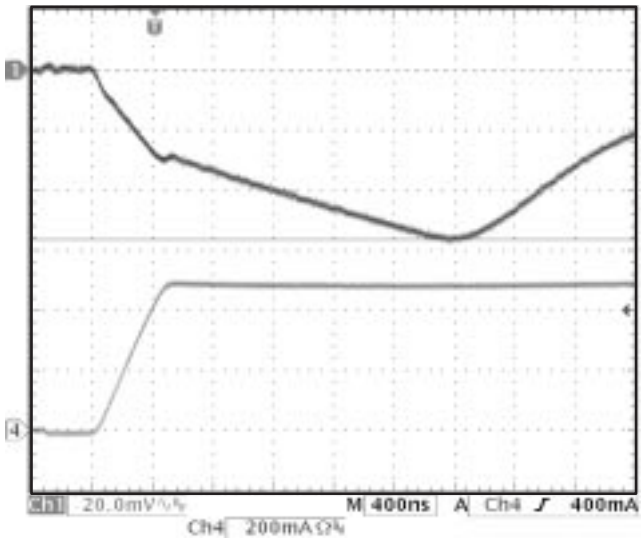
The load transient settling time of the LDO is approximately 1.5 ms.

Figure 4–2. No Load – Full Load (500 mA) Transition With C_O = 33 µF POSCAP™ – LDO Response Time



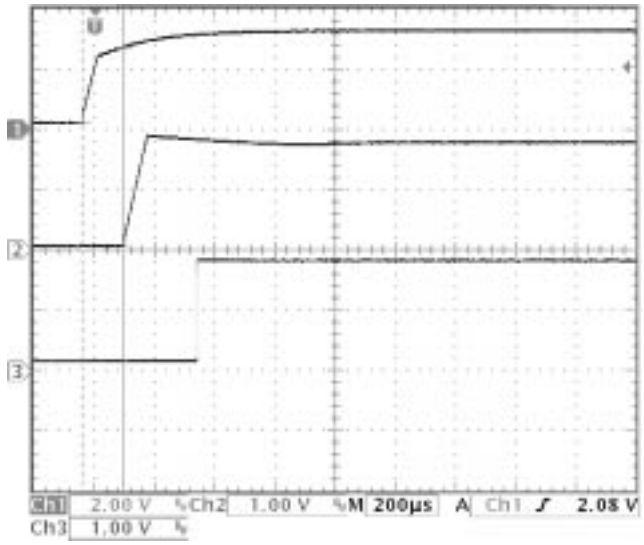
The load current rise time is 336 ns and the amplifier response time is approximately 2.4 µs.

Figure 4–3. No Load – Full Load (500 mA) Transition With C_O = 33 µF POSCAP™ – Maximum Transient Droop Voltage



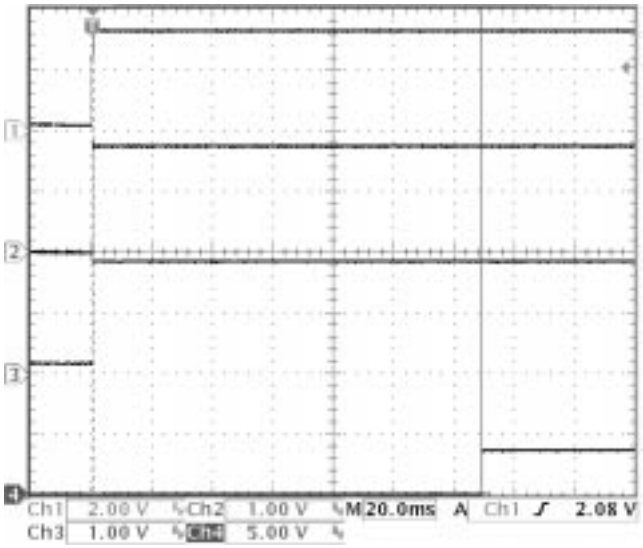
The maximum transient droop voltage is 56 mV.

Figure 4–4. Timing When SEQUENCE = Low



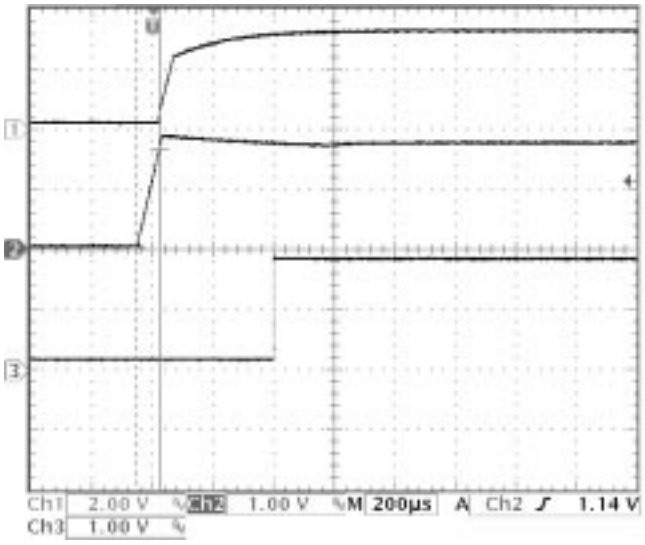
$V_{IN1} = V_{IN2}$ at 5V and both V_{OUT1} (CH1) and V_{OUT2} (CH2) have no load. $\overline{EN}$ is pulsed with a fast pulse. V_{OUT1} powers up before V_{OUT2} when SEQUENCE = low. PG_1 (CH3), tied to $\overline{MR1}$, goes high when V_{OUT1} reaches 95% of regulated voltage.

Figure 4–5. Timing When SEQUENCE = Low, Including $\overline{RESET}$



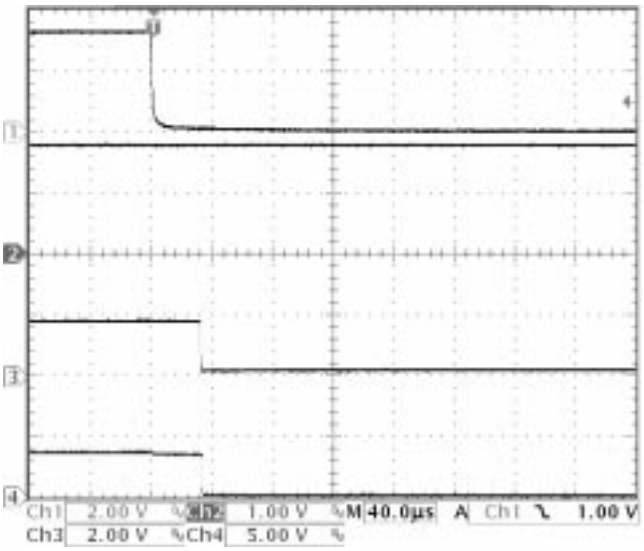
$V_{IN1} = V_{IN2}$ at 5V and both V_{OUT1} (CH1) and V_{OUT2} (CH2) have no load. $\overline{EN}$ is pulsed with a fast pulse. V_{OUT1} powers up before V_{OUT2} when SEQUENCE = low. PG_1 (CH3), tied to $\overline{MR1}$, goes high when V_{OUT1} reaches 95% of regulated voltage. After a 120 ms delay, $\overline{RESET}$ (CH4) is being driven by both V_{OUT1} and V_{OUT2} power good.

Figure 4–6. Timing When SEQUENCE = High



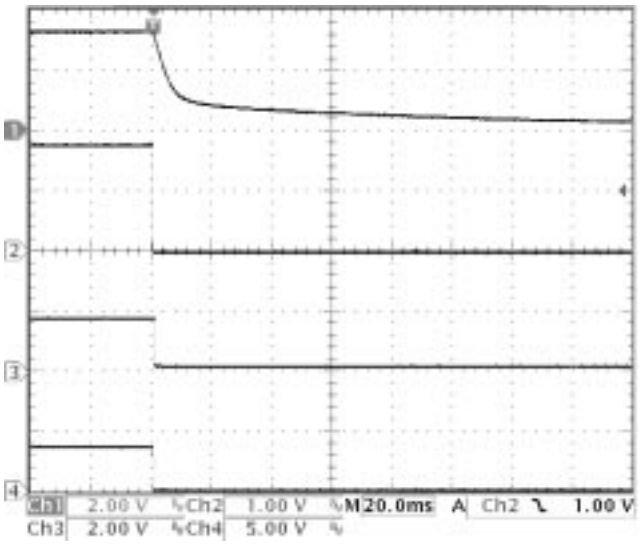
$V_{IN1} = V_{IN2}$ at 5V and both V_{OUT1} (CH1) and V_{OUT2} (CH2) have no load. $\overline{EN}$ is pulsed with a fast pulse. V_{OUT2} powers up before V_{OUT1} when SEQUENCE = high. PG_1 (CH3), tied to $\overline{MR1}$, goes high when V_{OUT1} reaches 95% of regulated voltage.

Figure 4–7. Timing When SEQUENCE = High and V_{OUT1} Faults Out



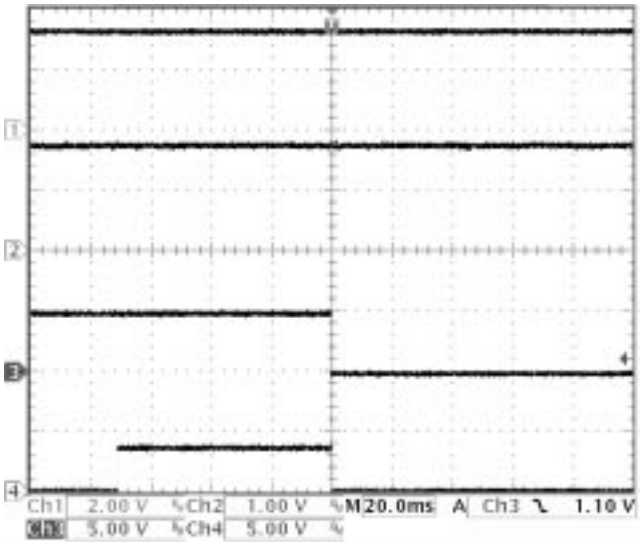
When SEQUENCE = high, V_{OUT2} (CH2) remains on even after V_{OUT1} (CH1) faults out due to current limit. The V_{OUT1} fault causes PG_1 (CH3), tied to $\overline{MR1}$, to go low. $\overline{MR1}$ causes $\overline{RESET}$ (CH4) to go low.

Figure 4–8. Timing When SEQUENCE = High and V_{OUT2} Faults Out



When SEQUENCE = high and V_{OUT2} (CH2) faults out due to current limit, V_{OUT1} (CH1) is disabled and PG_1 (CH3), tied to $\overline{MR1}$, goes low. The V_{OUT2} fault causes RESET (CH4) to go low.

Figure 4–9. Timing When $\overline{MR}$ Is Toggled



MR1 (CH3)is taken low and RESET (CH4) follows $\overline{MR1}$. V_{OUT1} (CH1) and V_{OUT2} (CH2) are unaffected.

All results are consistent with those reported in the SLVS222 datasheet.